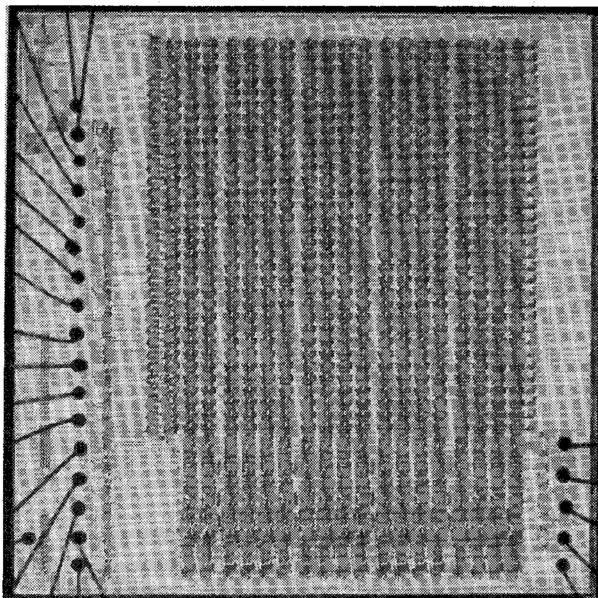

Fig. 5. A fault-tolerant CAM component.

IV. Results

To validate the design of the basic component and the fault-tolerance mechanism, prototype components were fabricated on a 5-μm polysilicon-gate NMOS process: a 16×64-bit component (4.53×3.56 mm, 10 354 transistors) of the basic CAM design, and an 18×64-bit component (4.72×4.35 mm, 11 875 transistors; see Fig. 5) with the fault-tolerance mechanism. Both components were verified by functional testing, and the mechanism was shown to work.

By using principles and techniques already within the basic component design, it has been possible to exploit the natural fault tolerance of CAM's at a cost of one extra latch per word which, in the prototype realization, represents an increase of only 4 percent in word area. The tolerance is effective against defects in the shift-register words which occupy over 75 percent of the word area in the basic component.

Acknowledgment

The author would like to thank the members of the Integrated Systems Group of the University of Edinburgh, Electrical Engineering Department, especially Dr. P. B. Denyer, for their assistance and encouragement.

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On the Analysis and Design of CMOS-Bipolar SRAM's

HECTOR DE LOS SANTOS AND BERND HOEFFLINGER

***Abstract*—The design and operation of a CMOS-bipolar SRAM cell, which incorporates cross-coupled CMOS and n-p-n access transistors, is discussed. A column circuitry to accompany this cell is proposed. Simulation results attributing column access time, standby power dissipation, and active power dissipation of 6–8 ns, 6.5 nW/bit, and 4 mW/bit, respectively, for a cell area of ~ 450 μm^2, suggest the suitability of this approach for applications requiring density, performance, and moderate power.**

I. Introduction

The main issues governing the design of high-performance memories are the following [1]: standby power dissipation, operating power dissipation, access time, loading effect of memory cells on address lines, and cell area.

It is found in practice that compromises must be reached as conflicts exist which preclude the optimization of all of the above simultaneously. For instance, the cell size of a static CMOS RAM cell is determined by the minimum feature size and the noise margin; the noise margin depends on the conductance ratio of the inverter transistor and the access transistor; and the conductance ratio also partly determines the speed performance and the power dissipation of the RAM [2]. However, while the optimization of power dissipation, loading, and cell area dictates a small aspect-ratio inverter, as well as small access and bit-load transistors, improved speed requires relatively large inverter and access transistors.

At the cell level, the power dissipation and area problems have been addressed through the incorporation of polysilicon resistors replacing the P-load devices. At the column level, both speed and power have been enhanced through the use of reduced logic swings and new equalization techniques as applied to the pertinent bit-line pairs, data-line pairs, and output path upon an address change [3].

The recent development of high-performance CMOS-bipolar processes [4], [5] has provided the capability for fabricating SRAM's in which the best of both technologies is at the designer's disposal [6].

In this paper, one CMOS-bipolar SRAM concept [7] is evaluated. Section II relates to the operation of the CMOS-bipolar cell. Section III describes the design considerations of the cell. Sections IV and V compare and discuss the performance of both cell and output path circuitry. Finally, Section VI discusses timing considerations for fastest READ time.

II. CMOS-Bipolar Cell Operation

The cell schematic and READ/WRITE timing diagrams are shown in Fig. 1. To read the cell's contents, the rising of V_1 causes the node storing a logic ONE to rise towards V_1 through the associ-

Manuscript received July 21, 1986; revised March 20, 1987. This work was supported by a grant from VTC Inc., Minneapolis, MN.

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IEEE Log Number 8715172.

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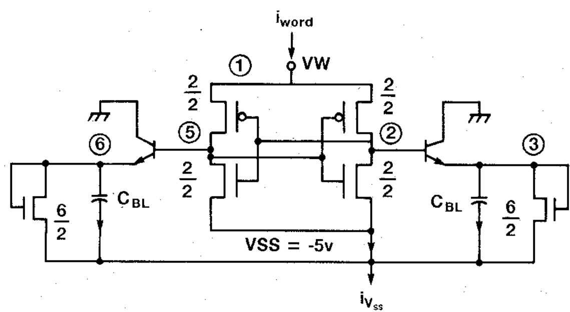

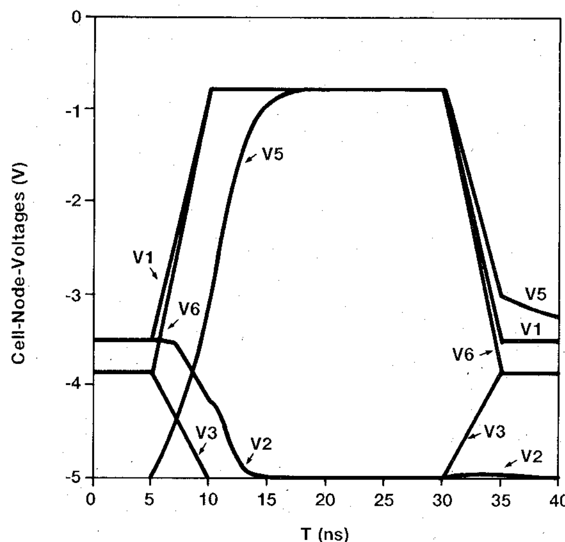

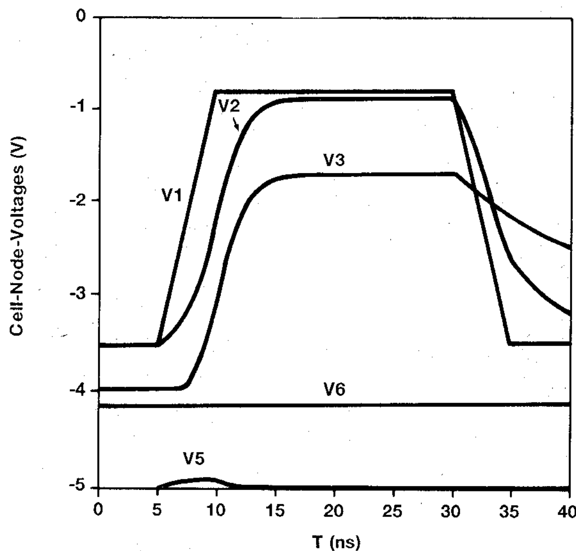

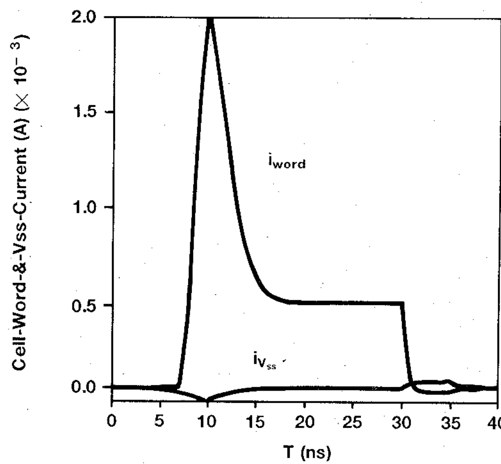

Fig. 1. CMOS-bipolar SRAM: (a) cell, (b) READ cycle, (c) WRITE cycle, and (d) cell current.

ated PMOS load device. The result of this is to forward bias the corresponding bipolar pass transistor, which then charges the bit line to one diode drop below V_1. The other storage node remains at logic ZERO, keeping the corresponding pass transistor cut off. Writing a logic ONE into a given storage node is accomplished by forcing the bit line corresponding to the opposite storage node to logic ZERO. The speed limitations on this cell are posed by the ability to turn on a given pass bipolar transistor. If the bipolar transistors are properly biased, then the READ speed will depend both on the bit-line capacitance and on the rise time of the word-line driver.

III. Cell Design

The design of the CMOS-bipolar cell consists of choosing the P-load devices to be minimum size. Since the N-driver devices are not required to discharge the bit-line capacitance, they are chosen to be minimum size also, in contrast to a pure CMOS cell. The bipolar pass transistors are chosen to have a minimum size in order to reduce the capacitive loading of the pull-up devices and hence reduce the switching time of the cell. For a given expected bit-line capacitance C_{BL}, an optimal emitter length $L_{E_{opt}}$ can be found [8]. The bit-line load is chosen to set the bit-line voltage between -3.5 and -4.2 V, which are the voltage levels at which the bipolar pass transistor whose base is storing a logic ONE will be in cutoff and in equilibrium, respectively. Its size determines the recovery time for the bit line to return to its quiescent voltage after the word-line pulse is removed. The quiescent bit-line voltage will ultimately be a function of the threshold voltage as well as the subthreshold characteristics of the bit-line load.

IV. Intrinsic Cell: Evaluation

A. Standby Power Dissipation

The standby power of the CMOS-bipolar cell is determined by the leakage current of the P loads and the cutoff currents of the bipolar pass transistors. However, the fact that in standby the cell supply is reduced to 1.5 V improves its performance in this respect (see Fig. 1(d)).

B. Active Power Dissipation

In the CMOS-bipolar cell, the bulk of the power (Fig. 1(d)) is dissipated during cell selection. At the array level, the power dissipation problem is compounded since, in selecting a given cell, power must be expended in bringing all the cells in the given

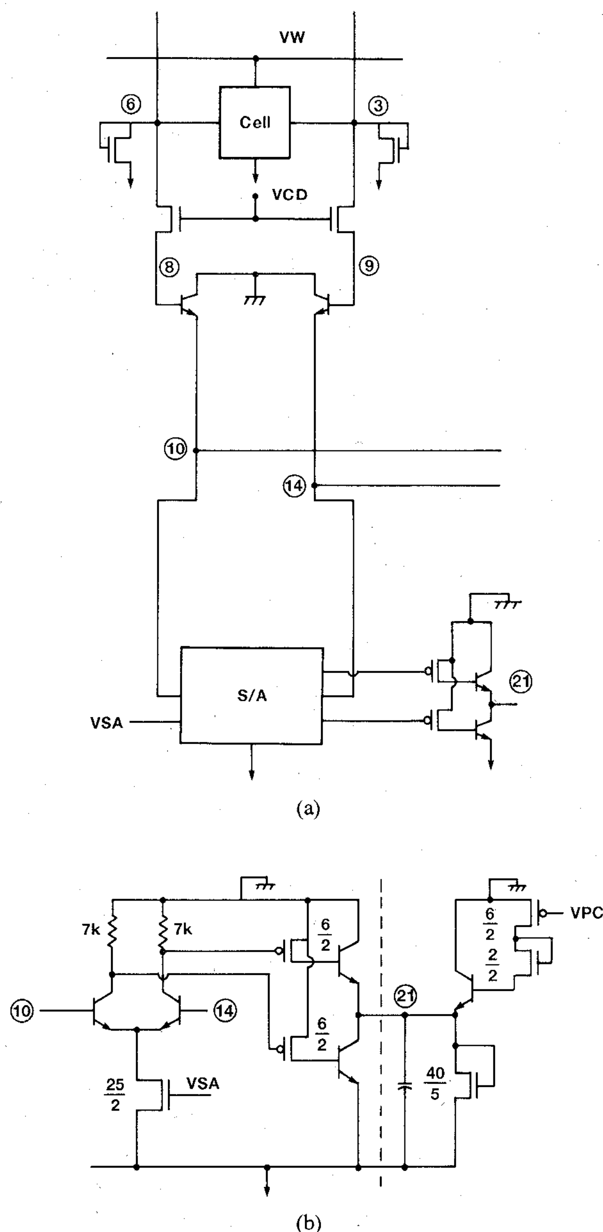

Fig. 2. CMOS-bipolar SRAM: (a) column organization, and (b) sense amplifier.

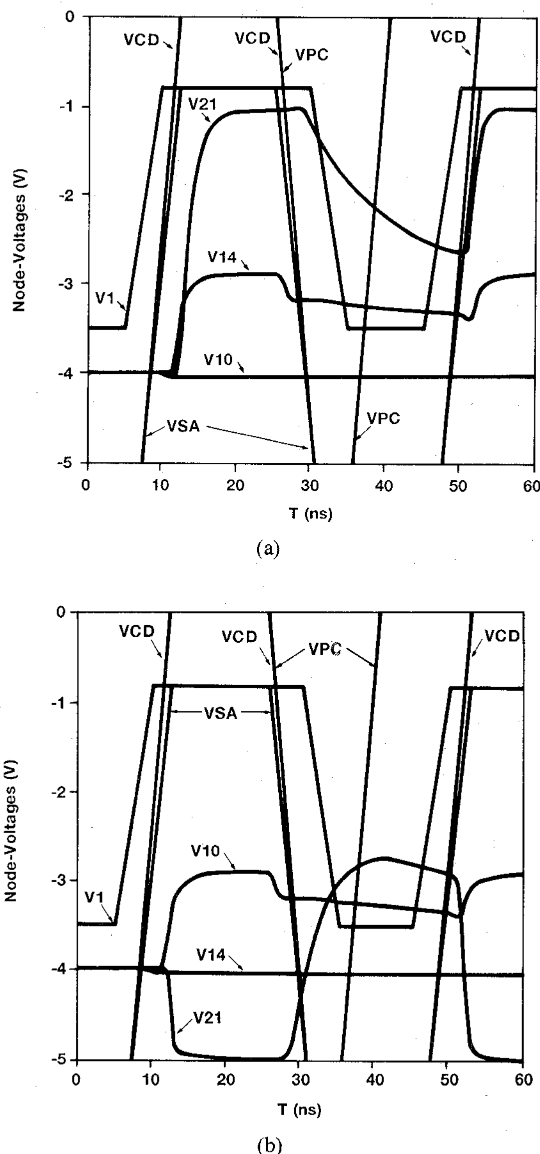

Fig. 3. CMOS-bipolar SRAM: (a) reading a ONE, and (b) reading a ZERO.

row from the standby voltage of 1.5 V to the active-mode voltage of 4.2 V with the accompanying fact that the bipolar pass transistors are also turned on (see Fig. 1(c)). The divided-word-line arrangement is suggested [9].

C. Access Time

Because the pass transitor of the CMOS-bipolar cell is a bipolar one biased halfway between cutoff and equilibrium, its access time is virtually determined by the bit-line capacitance, the rise time of the word-line driver, and the bipolar transistor's high transconductance (see Fig. 3(a)).

D. Write Time

The WRITE time of the CMOS-bipolar cell is a function of the charge and discharge of the bit lines, both of which force the switching of the cell through the capacitive coupling to the storage nodes provided by the base–emitter capacitors (see Fig. 1(c)).

V. OUTPUT PATH CIRCUITRY

The proposed column circuitry of the CMOS-bipolar SRAM is shown in Fig. 2.

The bias conditions of the bipolar pass transistors for highest speed of response and minimum power dissipation, together with the word-line swing, determine the maximum differential bit-line voltage. This turns out to have a magnitude of ~ 2 V (see Fig. 1(b)). As a consequence, there is no need for a pseudo-column sense amplifier. The column circuit terminates in the column-select pass transistors and data-bus driver transistors. These data-bus driver transistors are chosen to be bipolar transistors and are also biased for reduced turn-on delay.

The main data-line sense amplifier is a simple emitter-coupled comparator which, like its CMOS counterpart, is clocked [3]. However, as seen in Fig. 3, during a READ operation only one of the emitter-coupled transistors can be turned on since only one of the bit lines changes. This, together with the fact that the PMOS transistor size is chosen such that its current $I_{D\infty}$ is close to the knee current I_K of the bipolar transistor, results in a very fast response. Double-to-single-ended conversion is accomplished by connecting the PMOS-bipolar push–pull as shown in Fig. 2(b).

TABLE I

Classification	CMOS/Bipolar	CMOS
Standby power (nW/bit)	6.51	0.32
Active power (mW/bit)	4.0	0.34
Access time (ns)	6-8	11.5 - 13.5
Loading to bit line	$C_{GS}+C_{BE}+C_{BC}$	C_{GS}
Loading to word line	$C_{BE}+C_{BC}+\frac{C_{BL}}{\beta}$	$2C_{0X}$
Cell area (μm^2)	$\simeq 450$	297.5

The output of this circuit is normally precharged to between -3.8 and -4.2 V, so the nature of the data being detected translates into a pull-up or pull-down transient. The CMOS-bipolar push–pull must be followed by a latch.

VI. Timing Considerations

The timing diagram is shown in Fig. 3. The control signals are the column select V_{CD}, the row select V_W, the sense-amplifier enable V_{SA}, and the precharge signal V_{PC}. Assuming a transition time of 5 ns for each signal, the column and sense-amplifier enable signals are delayed 2.5 ns with respect to the row-select signal. This minimizes the capacitive load to the cell during the initial stages of the bit-line charging transient and results in overall highest speed since the rest of the column circuit gets activated during the high slew portion of the transient. Particular care must be taken in not enabling the sense amplifier too early because this would cause the emitter-coupled bipolar transistors to turn on, hence introducing a delay due to the switching of the bias current from one transistor to the other. By considering the column circuits discussed so far, and assuming bit-line and data-bus capacitances of 3.5 pF [3], a quantitative assessment of important performance parameters has been carried out with the help of SPICE2G simulations, with device parameters typical of an advanced CMOS-bipolar technology [8]. The resulting performance parameters are indicated in Table I.

VII. Conclusions

A CMOS-bipolar memory concept has been studied regarding the factors determining its performance with respect to operating speed, power dissipation, and occupied area. Concerning the operating speed, it has been found that, for an advanced CMOS-bipolar technology, the column circuit exhibits an excellent performance, namely, an access time of the order of 6–8 ns. This is a result of its fundamental mode of operation. The fact that the word line is capacitively coupled to the bit lines results in both a faster response time and a larger voltage swing. This last feature makes it possible to apply the bit-line differential signal (almost) directly to the column sense amplifier eliminating the need for an intermediate pseudo-column sense amplifier. Based on the results obtained via SPICE.2G simulations, it is expected that the CMOS-bipolar memory will have a power dissipation of about 6.5 nW/bit in the standby mode and about 4 mW/bit in the active mode. Because the driver transistors in the cell do not interact with the bit lines, they can be chosen to be minimum size. The major contribution to the cell area comes from the bipolar pass transistors. Their optimum size is a function of the bit-line capacitance.

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Noise-Generation Analysis and Noise-Suppression Design Techniques in Megabit DRAM's

Y. ITOH, K. NAKAGAWA, K. SAKUI, F. HORIGUCHI, AND M. OGURA

Abstract—**This correspondence reports a detailed noise-generation model of peak current and voltage-bouncing noise for DRAM's. This model was found to be a very effective tool for predicting and analyzing quantitative bouncing noise level in noise-suppressed circuit design, especially for high-performance high-density DRAM's. The resulting performance for the fabricated NMOS 1-Mbit DRAM is 100-mA peak current, 6-mA/ns current transition rate, and 0.27-V output voltage-bouncing noise for a standard system board.**

I. Introduction

Peak current and dI/dt (the derivative of current with respect to time) are important parameters for actual board and circuit design for DRAM's [1]–[4]. The peak current increases the electromigration problem and IR drop. The large dI/dt induces the voltage-bouncing noises due to wiring inductance which degrades the power-supply margin and induces misfunctions in the peripheral circuits. These problems become more serious in high-density integration, such as in megabit DRAM's, because the ac power for charging and discharging the bit-line capacitors increases in proportion to the memory cell integration.

From this point of view, this correspondence describes a detailed noise-generation model, where the peak current and the dI/dt noise are simulated accurately. Employing this model, we

Manuscript received July 14, 1986; revised January 5, 1987.

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IEEE Log Number 8714879.